What is claimed is:

1. A hetero-junction bipolar transistor comprising:

an n-type sub-collector layer that is made of GaAs;

an n-type first collector layer that is made of a semiconductor material with a smaller avalanche coefficient than an avalanche coefficient of the sub-collector layer and that is formed on the sub-collector layer;

a second collector layer that is made of one of n-type and i-type GaAs with lower dopant concentration than dopant concentration of the sub-collector layer and that is formed on the first collector layer;

a p-type base layer that is made of GaAs and that is formed on the second collector layer; and

an n-type emitter layer that is made of a semiconductor material with a larger band gap than a band gap of the base layer and that is formed on the base layer.

2. The hetero-junction bipolar transistor according to Claim 1,

wherein a dopant concentration of the first collector layer is $1 \times 10^{17} cm^{-3}$ or more.

3. The hetero-junction bipolar transistor according to Claim 1,

wherein a thickness of the first collector layer is under 200nm.

4. The hetero-junction bipolar transistor according to Claim 1,

wherein a dopant has a concentration characteristic where the concentration becomes lower in direction from an interface between the first collector layer and the sub-collector layer to an interface between the first collector layer and the second collector layer.

5. The hetero-junction bipolar transistor according to Claim 1, further comprising a semiconductor layer that is formed between the first collector layer and the second collector layer,

wherein the semiconductor layer reduces discontinuity of a conduction band between the first collector layer and the second collector layer.

6. The hetero-junction bipolar transistor according to Claim 5,

wherein the semiconductor layer is an n-type spacer layer that is made of the same semiconductor material as the first collector layer or the second collector layer, and the semiconductor layer has a dopant concentration of $1 \times 10^{18} cm^{-3}$ or less.

7. The hetero-junction bipolar transistor according to Claim 1,

wherein the first collector layer is made of $In_xGa_{1-x}P$ ($0.47 \leqq x \leqq 0.52$).

8. The hetero-junction bipolar transistor according to Claim 7,

wherein the first collector layer has a disordered structure.

9. The hetero-junction bipolar transistor according to Claim 1,

wherein the emitter layer is made of $In_xGa_{1-x}P$ ($0.47 \leqq x \leqq 0.52$).

10. The hetero-junction bipolar transistor according to Claim 1,

wherein the first collector layer is made of $Al_yGa_{1-y}As$ ($0 \leqq y \leqq 1$).

11. The hetero-junction bipolar transistor according to Claim 10,

wherein a composition ratio y of Al in the first collector layer gradually changes in direction from the interface between the first collector layer and the sub-collector layer to the interface between

the first collector layer and the second collector layer.

12. The hetero-junction bipolar transistor according to Claim 10, wherein the emitter layer is made of $Al_yGa_{1-y}As$ ($0 \leqq y \leqq 1$).

13. The hetero-junction bipolar transistor according to Claim 5, wherein the semiconductor layer includes:

an n-type first spacer layer that is made of the same semiconductor material as the first collector layer, has a dopant concentration of $1 \times 10^{18} cm^{-3}$ or less and is in contact with the first collector layer; and

an n-type second spacer layer that is made of the same semiconductor material as the second collector layer, has a dopant concentration of $1 \times 10^{18} cm^{-3}$ or less and is in contact with the second collector layer.

14. A manufacturing method of a hetero-junction bipolar transistor, comprising:

a first step of laminating a sub-collector layer, a first collector layer, a first spacer layer, a second spacer layer, a second collector layer, a base layer and an emitter layer on a semiconductor substrate in this sequence;

a second step of etching a predetermined region in the emitter layer with a first etchant;

a third step of etching the base layer, the second collector layer and the second spacer layer with a second etchant using the etched emitter layer as a mask; and

a fourth step of etching, with a third etchant, predetermined regions in the first spacer layer and the first collector layer exposed by the etching with the second etchant.

15. The manufacturing method of the hetero-junction bipolar

transistor according to Claim 14,

wherein each of the sub-collector layer, the base layer, the second collector layer and the second spacer layer is made of GaAs to which a dopant is doped, and each of the first collector layer and the first spacer layer is made of InGaP to which a dopant is doped,

the second etchant in the third step is a mixed solution of phosphoric acid, hydrogen peroxide and water, and

the third etchant in the fourth step is hydrochloric acid diluted with water.

16. The manufacturing method of the hetero-junction bipolar transistor according to Claim 14,

wherein the hetero-junction bipolar transistor further includes an emitter cap layer, an emitter contact layer, an emitter electrode, a collector electrode and a base electrode,

the first step includes:

a first sub-step of laminating the emitter cap layer and the emitter contact layer on the emitter layer in this sequence; and

a second sub-step of etching predetermined regions in the emitter cap layer and the emitter contact layer with a fourth etchant, and

the manufacturing method of the hetero-junction bipolar transistor further comprises:

a fifth step of forming the collector electrode on the sub-collector layer exposed by the etching with the third etchant; and

a sixth step of forming the emitter electrode on the emitter layer exposed by the etching with the fourth etchant, and forming the base electrode on the emitter contact layer exposed by the etching with the fourth etchant.

17. The manufacturing method of the hetero-junction bipolar

transistor according to Claim 16,

wherein the hetero-junction bipolar transistor has a stepped surface,

a third step layer that constitutes the stepped surface is formed by etching the predetermined regions in the emitter cap layer and the emitter contact layer in the second sub-step,

a second step layer that constitutes the stepped surface is formed by etching the emitter layer that exists outside an outer edge of the third step layer in the second step and by etching the base layer, the second collector layer and the second spacer layer using said etched emitter layer as the mask in the third step, and

a first step layer that constitutes the stepped surface is formed by etching the first spacer layer and the first collector layer that exist outside an outer edge of the second step layer in the fourth step.